UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,320	06/24/2003	Peter T. Larsen	80107.034US1	1015

7590 06/13/2006

LeMoine Patent Services
c/o PortfolioIP
P.O. Box 52050
Minneapolis, MN 55402

EXAMINER	
PATEL, HETUL B	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 06/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,320	LARSEN, PETER T.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-10,13-16,19-24 and 26-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-10,13-16,19-24 and 26-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the communication filed on May 05, 2006. Claim 18 is cancelled; and claims 1, 2, 7, 10, 13, 14, 19, 20, 22, 23, 26 and 28 are amended. Claims 1-3, 5-10, 13-16, 19-24 and 26-28 are currently pending in this application.

2. Applicant's arguments filed on May 05, 2006 have been fully considered but they are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims1-3, 5-10, 19-24 and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Terauchi (USPN: 5,862,147) in view of Fandrich et al. (USPN: 5,353,256) hereinafter, Fandrich.

As per claim 1, Terauchi teaches a method of programming a FLASH memory device (i.e. the flash memory 21 in Figs. 1-2) comprising: issuing a blank check command (i.e. blank check operation) to a command register within the FLASH memory device (i.e. the flash memory 21 in Figs. 1-2), wherein the blank check command specifies a specified block to blank check (i.e. repeating the blank check steps for more

than one flash memories (blocks) on the wafer (memory device) (e.g. see Fig. 1)); and programming memory locations within the specified block (i.e. the portion) of the FLASH memory device (i.e. writing/programming only those addresses that verified as blank, see S41-S44 in Fig. 4). Furthermore, Terauchi teaches that in order to verify that the specified block is blank, the bit(s) where the result is written in the second memory area 23 in Fig. 2 is checked (e.g. see Col. 4, lines 36-58; Col. 5, lines 18-21 and Figs. 1-2 and 4).

However, Terauchi does not teach that in order to verify that the specified block is blank, a single bit in a status register within the FLASH memory is checked. Fandrich, on the other hand, teaches a flash memory device having a plurality of flash array blocks and a block status register circuit containing a block status register for storing a block status for each flash array block (e.g. see the abstract). Fandrich also teaches that the bits of the block status register indicates whether or not the block erase operation on a specified block is completed, i.e. verifying the specified block is blank (e.g. see Col. 1, lines 30-36). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the teaching of Fandrich in the method taught by Terauchi so it will provide the global status information for the entire flash memory device to the user from the flash memory device and no separate/secondary memory area is required to store it.

As per claim 2, the combination of Terauchi and Fandrich teaches the claimed invention as described above and furthermore, Fandrich teaches about checking a busy

bit in the status register within the FLASH memory device adapted to signify that the single bit is valid (e.g. see Col. 1, lines 30-33).

As per claim 7, Terauchi teaches a method of blank checking and programming a FLASH memory device (i.e. the flash memory 21 in Figs. 1-2) comprising: receiving a blank check command (i.e. blank check operation) from a device (i.e. the microcomputer 24 in Fig. 2) external to the FLASH memory device, wherein the blank check command specifies a specified block to blank check (i.e. repeating the blank check steps for more than one flash memories (blocks) on the wafer (memory device) (e.g. see Fig. 1)); in response to the blank check command received from a device external to the FLASH memory device, reading a plurality of memory locations in the specified block of the memory device; and receiving data to be programmed in the at least one block. Furthermore, Terauchi teaches that in order to verify that the specified block is blank, the bit(s) where the result is written in the second memory area 23 in Fig. 2 is checked (e.g. see Col. 4, lines 36-58; Col. 5, lines 18-21 and Figs. 1-2 and 4).

However, Terauchi does not teach that in order to signify that the specified block is blank, a single bit in a status register within the FLASH memory is set, wherein the status register is visible to the device external to the FLASH memory device. Fandrich, on the other hand, teaches a flash memory device having a plurality of flash array blocks and a block status register circuit containing a block status register for storing a block status for each flash array block (e.g. see the abstract). Fandrich also teaches that the bits of the block status register indicates whether or not the block erase operation on a specified block is completed, i.e. verifying the specified block is blank

(e.g. see Col. 1, lines 30-36). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the teaching of Fandrich in the method taught by Terauchi so it will provide the global status information for the entire flash memory device to the user from the flash memory device and no separate/secondary memory area is required to store it. Fandrich also teaches that the status register is visible to the device (i.e. the I/O processor 332 in Fig. 2) external to the FLASH memory device (e.g. see Col. 3, lines 58-64 and Fig. 2).

As per claims 19-20, see arguments with respect to the rejection of claims 7 and 2, respectively. Claims 19 and 20 are also rejected based on the same rationale as the rejection of the claims 7 and 2, respectively.

As per claim 3, the combination of Terauchi and Fandrich teaches the claimed invention as described above and furthermore, Terauchi teaches that issuing a blank check command comprises: issuing a blank check setup command (i.e. step S42 in Fig. 4); and issuing a blank check confirm command (i.e. step S43 in Fig. 4) (e.g. see Col. 2, lines 36+ and Fig. 4).

As per claims 8, 21 and 27, see arguments with respect to the rejection of claim 3. Claims 8, 21 and 27 are also rejected based on the same rationale as the rejection of the claim 3.

As per claims 5 and 6, the combination of Terauchi and Fandrich teaches the claimed invention as described above and furthermore, Terauchi teaches that the method further comprising repeating the issuing, checking and programming steps for

more than one block in the memory device, i.e. repeating these steps for more than one and each flash memories (blocks) on the wafer (memory device) (e.g. see Fig. 1).

As per claims 22 and 28, see arguments with respect to the rejection of claims 5-6. Claims 22 and 28 are also rejected based on the same rationale as the rejection of the claims 5-6.

As per claim 9, the combination of Terauchi and Fandrich teaches the claimed invention as described above and furthermore, Terauchi teaches that reading a plurality of memory locations comprises reading each memory location in the at least one block (i.e. the block between the 'RESET' address and 'FULL' address specified) (e.g. see Col.2, lines 36+ and Fig. 5).

As per claim 10, the combination of Terauchi and Fandrich teaches the claimed invention as described above and furthermore, Fandrich teaches about setting a busy bit adapted to signify the FLASH memory device is busy; and clearing the busy bit after setting the single bit in the status register to specify that the specified block is blank, i.e. the bits of the block status register indicates whether or not the block erase operation on a specified block is completed, so if the erase function is not finished, then it will set the bit one way indicating it's busy; and if the erase function is finished, then it will set the bit other way indicating the busy is cleared (e.g. see Col. 1, lines 30-36).

As per claim 23, Terauchi teaches an electronic system comprising a direct conversion receiver (i.e. the pad 31f in Fig. 3 that receives the test control signals); a processor (i.e. 24 in Fig. 2) coupled to the direct conversion receiver; and a memory device (i.e. 21 in Fig. 2) coupled to the processor, the memory device including a

FLASH memory core (i.e. 22 in Fig. 2) and a control block (the combination of 24 and 25 in Fig. 2) adapted to blank check a specified block of the FLASH memory core; and an external interface (i.e. 61 in Fig. 6) to allow communication between the control block and the processor, the external interface including a command register (i.e. the R1 and R2 in Fig. 6) to receive a blank check command that specifies the specified block (i.e. by plugging different values for R1 and R2 in Fig. 6), wherein the control block is capable of blank checking the specified block of the FLASH memory core during a programming operation by the processor, and wherein the control block is further capable of asserting a signal on a conductor external to the memory device to signify that the specified block is blank (e.g. see Col. 4, lines 36-58; Col. 5, lines 18-21; Col. 6, lines 13+ and Figs. 2-3 and 6).

However, Terauchi does not teach that the external interface including a status register having a bit to signify that the specified block is blank. Fandrich, on the other hand, teaches the external interface (i.e. the interface circuit 40 in Figs. 3-4a) including a status register (i.e. the block status register (BSR) 216 in Fig. 4a) (e.g. see Figs. 3-4a). Fandrich also teaches that the bits of the block status register indicate whether or not the block erase operation on a specified block is completed, i.e. signifying the specified block is blank (e.g. see Col. 1, lines 30-36). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the teaching of Fandrich in the method taught by Terauchi so it will provide the global status information for the entire flash memory device to the user from the flash memory device and no separate/secondary memory area is required to store it.

As per claim 24, the combination of Terauchi and Fandrich teaches the claimed invention as described above and furthermore, Terauchi teaches that the control block comprises a microcontroller (i.e. the microcomputer 24 in Fig. 2).

As per claim 26, Terauchi teaches an electronic system comprising a direct conversion receiver (i.e. the pad 31f in Fig. 3 that receives the test control signals); a FLASH memory device (i.e. 21 in Fig. 2); a processor (i.e. 24 in Fig. 2) coupled to the direct conversion receiver and the FLASH memory device wherein the blank check command specifies a specified block to blank check (i.e. repeating the blank check steps for more than one flash memories (blocks) on the wafer (memory device) (e.g. see Fig. 1)); and programming memory locations within the specified block (i.e. the portion) of the FLASH memory device (i.e. writing/programming only those addresses that verified as blank, see S41-S44 in Fig. 4). Furthermore, Terauchi teaches that in order to verify that the specified block is blank, the bit(s) where the result is written in the second memory area 23 in Fig. 2 is checked (e.g. see Col. 4, lines 36-58; Col. 5, lines 18-21 and Figs. 1-2 and 4).

However, Terauchi does not teach that in order to verify that the specified block is blank, a single bit in a status register within the FLASH memory is checked. Fandrich, on the other hand, teaches a flash memory device having a plurality of flash array blocks and a block status register circuit containing a block status register for storing a block status for each flash array block (e.g. see the abstract). Fandrich also teaches that the bits of the block status register indicates whether or not the block erase operation on a specified block is completed, i.e. verifying the specified block is blank

(e.g. see Col. 1, lines 30-36). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the teaching of Fandrich in the method taught by Terauchi so it will provide the global status information for the entire flash memory device to the user from the flash memory device and no separate/secondary memory area is required to store it.

4. Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shokouhi (USPN: 6,651,199) in view of Fandrich.

As per claim 13, Shokouhi teaches a memory device (i.e. 100 in Figs. 2-3A) comprising: a FLASH memory core (i.e. the memory circuit 120 in Figs. 2-3A); a control block (i.e. 110 in Fig. 2) adapted to blank check at least a portion of the FLASH memory core; and an external interface (i.e. 110 in Fig. 2) to allow communication between the control block and a device (i.e. the JTAG-based operating system) external to the memory device, the external interface including a command register (i.e. the R1 and R2 in Fig. 6) to receive a blank check command that specifies the specified block (i.e. by plugging different values for R1 and R2 in Fig. 6), wherein the control block is capable of blank checking the specified block of the FLASH memory core during a programming operation when the memory device is in use in a system (e.g. see Col. 4, lines 36-58; Col. 5, lines 18-21; Col. 6, lines 13+ and Figs. 2-3 and 6).

However, Shokouhi does not teach that the external interface including a status register having a bit to signify that the specified block is blank. Fandrich, on the other hand, teaches the external interface (i.e. the interface circuit 40 in Figs. 3-4a) including

a status register (i.e. the block status register (BSR) 216 in Fig. 4a) (e.g. see Figs. 3-4a). Fandrich also teaches that the bits of the block status register indicate whether or not the block erase operation on a specified block is completed, i.e. signifying the specified block is blank (e.g. see Col. 1, lines 30-36). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the teaching of Fandrich in the method taught by Shokouhi so it will provide the global status information for the entire flash memory device to the user from the flash memory device and no separate/secondary memory area is required to store it.

As per claim 14, the combination of Shokouhi and Fandrich teaches the claimed invention as described above and furthermore, Fandrich teaches that the status register (i.e. the 216 in Fig. 4a) includes a second bit (the status bit) to signify that the memory device is busy (i.e. when the erase function is not completed (e.g. see Col. 1, lines 30-36 and Fig. 3-4a).

As per claim 15, the combination of Shokouhi and Fandrich teaches the claimed invention as described above and furthermore, Shokouhi teaches that the control block comprises a state machine (i.e. 320 in Fig. 4) (e.g. see Figs. 4 and 6).

As per claim 16, the combination of Shokouhi and Fandrich teaches the claimed invention as described above and furthermore, Shokouhi teaches that the control block comprises a microcontroller (i.e. 220 in Fig. 3A).

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HBP
HBP

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100